PhD Dissertations – *all students received support from his research grants*

1. Krishna Gnawali, Emerging Memory-based Designs and Resiliency to Radiation Effects, School of Electrical Computer and Biomedical Eng., SIUC, October 2020. Employed at Synopsys Corp., Mountain View, CA.
2. Basim Shanyour, Testing and Security considerations in the presence of process variations, ECE Dept.., SIUC, March 2020. Currently with Qualcomm Corporation, San Diego, CA
3. Pavan Kumar Javvaji, Statistical Methods for Critical Path Selection and Fault Coverage in Integrated Circuits, ECE Dept.., SIUC, May 2019. Currently with Nvidia Corporation, Santa Clara, CA.
4. Wisam Al-Jubouri, Measuring the Delay of Embedded Segments in Integrated Circuits using Current Sensors, ECE Dept.., SIUC, October 25, 2018. Currently with Cadence, NY.
5. Seyed Nima Mozaffari, Design and Test of Digital Circuits and Systems Using CMOS and Emerging Resistive Devices, ECE Dept., SIUC, March 2018. Currently with Nvidia Corp., Santa Clara, CA.
6. Adam Watkins, Analysis and Mitigation of Multiple Radiation Induced Errors in Modern Circuits, ECE Dept., SIUC, November 2016. Currently with Amazon, Space and Radiation, Seattle, WA.
7. Joseph Lenox, Parallel and Fault Grading Heuristic and Testing Approaches to Trojan IC Detection, ECE Dept., SIUC, October 2016. Currently with Collins Aerospace, Cedar Rapids, IA.
8. Luke Pierce, Testing and Security Related Considerations in Embedded Software, ECE Dept., SIUC, August 2016. Currently with Amazon Web Services, Portland, OR.
9. Phaninder Alladi, Validation of Circuit Timing Behavior in the Presence of Delay Defects and NBTI aging, ECE Dept., SIUC, August 2016. Synopsys Corporation, Mountain View, CA. Currently with Walmart, AR
10. Ahish Mysore Somashekar, Methodologies for Test and Diagnosis of Delay Defects in Integrated Circuits, ECE Dept., SIUC, December 2015. Currently with Intel Corporation, Santa Clara, CA.
11. Pragyan (Sheela) Mohanty, Function-based Algorithms for Biological Sequences, ECE Dept., SIUC, December 2015. Currently with Sierra Nevada Corporation, Reno, NV.
12. Chandra Babu Dara, Design for High Performance Threshold Logic Gates, ECE Dept., SIUC, December 2015. Currently with Broadcom Corporation, San Jose, CA.
13. Ashok Kumar Palaniswamy, Synthesis and Testing of Threshold Logic Circuits, ECE Dept., SIUC, July 2014. Currently with Synopsys Corporation, Mountain View, CA.
14. Kedar Karmakar, Scalable bus encoding for error-resilient high-speed on-chip communication, ECE Dept., SIUC, June 2013. Currently with Intel Corporation, Hillsboro, OR.
15. Sreenivas Gangadhar, Analytical Methods to Propagate and Diagnose Single Event Transients, ECE Dept., SIUC, August 2012. Currently with Intel Corporation, Austin, TX.
16. Dheepakkumaran Jayaraman, Optimization Techniques for Performance and Power Dissipation in Test and Validation, ECE Dept., SIUC, May 2012. Currently with Intel Corporation, Santa Clara, CA. (Previously with Nvidia, CA, Qualcomm, CA, Barefoot Networks, CA).
17. Manoj Kumar Goparaju, Coping with discrepancies of the manufactured weights in Threshold Logic gates, ECE Dept., SIUC, December 2009. Currently with Qualcomm, Raleigh, NC.
18. Michael N. Skoufis, Coping with delays and hazards in buses and random logic in deep sub-micron, ECE Dept., SIUC, August 2009. Currently with Sandia National Labs, NM. (Previously with Raytheon Inc., Tucson AZ).
19. Edward Flanigan, Scalable Test Generation for Path Delay Faults, ECE Dept., SIUC, January 2009. Currently with Northrop Grumman. (Previously with Boeing Corp., OK, and with Raytheon Inc., AZ).
20. Arkan Abdulrahman, Test Pattern Generation Techniques that target low Test Application Time, ECE Dept., SIUC, May 2008. Currently with Qualcomm Inc., San Diego, CA. (Previously with Marvell Inc., Phoenix, AZ).
21. Rajekhar Adapa, Techniques for Improved Diagnosis, ECE Dept., SIUC, May 2008. Currently with Qualcomm, San Jose, CA. (Previously with Nvidia, CA.)
22. Milir M. Vaseekar Kumar, ATPG and Fault Grading for Delay Faults, ECE Dept., SIUC, December 2006. Currently with Synopsys Inc., Mountain View, CA.
23. Khadija.J. Stewart, Emerging technologies Involving Networks, ECE Dept., SIUC, August 2006. Currently tenured Assoc. Professor, Computer Science Dept., Depauw University, Newcastle, IN
24. Mohammad Moiz Khan, Re-synthesis for Intellectual Property Protection and Performance, ECE Dept., SIUC, August 2006. Currently with Synopsys Inc., Mountain View, CA.
25. Saravanan Padmanaban, Non-enumerative techniques for delay verification and diagnosis, College of Engineering, SIUC, August 2003. Currently with Intel Corporation, Hillsboro, OR. (Previously with the ECE Dept., Univ. of Maryland Baltimore County.)

26. Maria Michael, Test-based timing verification using functional techniques, College of Engineering, SIUC, 2002. Currently tenured Assoc. Professor, ECE Dept., Univ. of Cyprus. (Previously Assist. Professor, CSE Dept., Univ. of Notre Dame.)
27. Dimitrios Karayiannis, Delay Considerations in Testing and Synthesis of Integrated Circuits, College of Science, SIUC, August 1996. Currently VP of R&D at Inside Secure, France. (Previously with Texas Instruments Inc., CA, Synopsys Inc., CA, and Viewlogic Inc., CA.)

co-Directed

28. Cheng Luo (Primary advisor W.-C. Hu, Computer Science Department), SIUC, 2007. Currently with Computer Science Department, Coppin State University, Baltimore, MD
29. Zhewei Jiang (Primary advisor: W.-C. Hu, Computer Science Department), SIUC, 2007. Currently with University of Maryland Baltimore County, Baltimore, MD.
30. Dimitri Kagaris (Primary advisor: F. Makedon), Computer Science Department, Dartmouth College, 1994. Currently with Electrical and Computer Engineering Department, SIUC.

Recent MS Theses (since 2014) – *all students received support from his grants*

- Aashish Itani, Comparison of Adversarial Robustness of ANN and SNN towards Black Box Attacks, May 2021. Currently with Intel, Santa Clara, CA.
- Chandra Sagili, Multi-threading accelerator for SMT based RTL verification, ECE Dept. SIUC, October 2019. Currently with Cadence, CA.
- Keerthana Samala, Test Pattern Generation for Double Transition Faults, May 2018. Currently an embedded systems software engineer with Valeant Pharmaceuticals.
- Damianos Veskoukis, Automatic MC/DC Test Pattern Generation, June 2018. Currently with Oxford University, UK (PhD program)
- Fatemeh Mohammadi Shakiba, CMOS-based implementation of hyperbolic tangent activation function for artificial neural network, March 2018. Currently with NJIT (PhD program).
- Ajitkumar Yadav, Fault Diagnosis in Failed Functional Sequences at RTL Level, ECE Dept., August 2016. Currently with AMD, Orlando, FL.
- Ehsan Ahmadi, Solving Incremental Specifications using Z3 SMT Solver, ECE Dept., SIUC, (August 2016). Currently with the Univ. of Wisconsin (PhD program).
- Theodore Toulas, Transition fault-driven delay defect diagnosis in the presence of process variations, ECE Dept., SIUC, December 2015. Currently with Synopsys, Mountain View, CA.
- Vasiliki Gkintzou, Preemptive edge-based scheduling for real-time networks on-a-chip, ECE Dept., SIUC, October 2014. Currently with Advantest, San Jose, CA.